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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,055	08/26/2003	Tapan J. Chakraborty	CHAKRABORTY 8-2	2959

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,055	CHAKRABORTY ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,18* is/are rejected.

7)☒ Claim(s) *16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

SECOND DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1,2,4,5,7-10,12,15,18 are rejected under 35 U.S.C. 102(e) as being anticipated by Nadeau-Dostie et al. (USPN 6536008B1). As per claim 1, Nadeau-Dostie et al. discloses a fault selection circuit adapted with fault selection data identifying selected circuit outputs of the circuit device, a fault value circuit adapted with fault values for injection on corresponding selected circuit outputs, and the fault selection circuit controlling the selected circuit outputs in place of control by system logic during injection of respective fault values in column 3, lines 14-20.

3. As per claim 2, Nadeau-Dostie et al. discloses the data and the fault values, respectively, are received from an industry standard, TAP controller in column 3, liens 11-13; column 4, lines 54-60.

4. As per claim 4, Nadeau-Dostie et al. discloses wherein, the circuits are independent of an operating system of the circuit device in Figures 5-17. There is no disclosed operating system in the circuits.

5. As per claim 5, Nadeau-Dostie et al. discloses wherein, the system selects pins for fault injection, and the pins are connected to a circuit board having circuit board interconnections being tested for vector verification by the fault injection values in column 3, lines 14-20; column 6, lines 20-47.

6. As per claim 7, Nadeau-Dostie et al. discloses wherein, the fault selection circuit comprises a user defined scan register in the circuit device in column 18, line 61 – column 19, line 6.

7. As per claim 8, Nadeau-Dostie et al. discloses the fault value circuit comprises a user defined scan register in the circuit device in column 7, lines 4-50; column 18, line 61 – column 19, line 6.

8. As per claim 9, Nadeau-Dostie et al. discloses the system selects an internal register for fault injection, and the internal register is in the system logic of the circuit device in column 7, lines 4-50.

9. As per claim 10, Nadeau-Dostie et al. discloses storing and updating fault injection selection data in a first register; scanning and storing fault injection values in a second register; and updating the fault injection selection data and the fault injection values at the selected fault injection locations of the programmable circuit device, while the selected fault injection locations are controlled by the first and second register instead of by system logic of the circuit device in column 7, lines 4-50.

10. As per claim 12, Nadeau-Dostie et al. discloses injecting stuck-at fault injection values on selected pins of the fault injection locations in column 7, lines 4-50.

11. As per claim 15, Nadeau-Dostie et al. discloses injecting stuck-at fault injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board in column 7, lines 4-50; column 18, line 61 – column 19, line 6.

12. As per claim 18, Nadeau-Dostie et al. discloses injecting one or more of the fault injection values at an internal register in the system logic of the circuit device in column 7, lines 4-50.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3,6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. in view of Davies (US Publication Number 20020199134A1).

15. As per claim 3, Nadeau-Dostie et al. fails to explicitly state the circuit device comprises a field programmable gate array, FPGA.

Davies discloses this limitation on page 1, paragraph 0003.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the circuit device comprises a field programmable gate array, FPGA. A person of ordinary skill in the art would have been motivated to have the circuit device comprises a field programmable gate array, FPGA because an FPGA is a type of integrated circuit that is tested.

16. As per claim 6, Nadeau-Dostie et al. fails to explicitly state the system selects pins for fault injection, the pins are connected to a backplane, and the backplane is coupled to a backplane test tool having a backplane test algorithm being tested for verification.

Davies discloses this limitation on page 1, paragraph 0005.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system select pins for fault injection, the pins are connected to a backplane, and the backplane is coupled to a backplane test tool having a backplane test algorithm being tested for verification. A person of ordinary skill in the art would have been motivated to have the system select pins for fault injection, the pins are connected to a backplane, and the backplane is coupled to a backplane test tool having a backplane test algorithm being tested for verification because backplane testing allows for diagnostic software to correctly identify faults induced on the backplane.

17. Claims 11,13,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nadeau-Dostie et al. in view of Abramovici et al. (USPN 6202182B1).

18. As per claim 11, Nadeau-Dostie et al. fail to explicitly state injecting stuck-on fault injection values on selected pins of the fault injection locations.

Abramovici et al. discloses this limitation in column 7, lines 16-26.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have injecting stuck-on fault injection values on selected pins of the fault injection locations. A person of ordinary skill in the art would have been

motivated to have injecting stuck-on fault injection values on selected pins of the fault injection locations because configuration memory bit faults are also detected.

19. As per claim 13, Nadeau-Dostie discloses injecting stuck-at fault injection values on selected pins of the fault injection locations in column 7, lines 4-50.

Nadeau-Dostie et al. fail to explicitly state injecting stuck-on fault injection values on selected pins of the fault injection locations.

Abramovici et al. discloses this limitation in column 7, lines 16-26.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have injecting stuck-on fault injection values on selected pins of the fault injection locations. A person of ordinary skill in the art would have been motivated to have injecting stuck-on fault injection values on selected pins of the fault injection locations because configuration memory bit faults are also detected.

20. As per claim 14, Nadeau-Dostie et al. fail to explicitly state injecting stuck-on fault injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board.

Abramovici et al. discloses this limitation in column 7, lines 16-26.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have injecting stuck-on fault injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board. A person of ordinary skill in the art would have been motivated to have injecting stuck-on fault

injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board because configuration memory bit faults are also detected.

Claim Objections

21. Claims 16,17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

22. Applicant's arguments with respect to the rejection(s) of claim(s) under 1-18 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new rejection is made for claims 1-15,18, as disclosed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yolanda L Wilson

Yolanda L Wilson
Examiner
Art Unit 2113